RL-TR-95-279
Final Technical Report
January 1996

$Si_{1-x}Ge_x/Si$ HETEROSTRUCTURES FOR INFRARED DETECTION

Princeton University

James C. Sturm

Rome Laboratory
Air Force Materiel Command
Rome, New York

This report has been reviewed by the Rome Laboratory Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RL-TR-95-279 has been reviewed and is approved for publication.

APPROVED: Maxwell Chi

MAXWELL CHI
Project Engineer

FOR THE COMMANDER: Robert V. McGahan

ROBERT V. MCGAHAN
Director
Electromagnetics & Reliability Directorate

If your address has changed or if you wish to be removed from the Rome Laboratory mailing list, or if the addressee is no longer employed by your organization, please notify RL (ERO) Hanscom AFB MA 01731. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	January 1996	Final Sep 93 - Sep 95

4. TITLE AND SUBTITLE

$SI_{1-x}GE_x$/SI HETEROSTRUCTURES FOR INFRARED DETECTION

5. FUNDING NUMBERS

C - F19628-93-K-0013
PE - 61102F
PR - 2305
TA - C1
WU - 10

6. AUTHOR(S)

James C. Sturm

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Princeton University
Department of Electrical Engineering
Princeton NJ 08544

8. PERFORMING ORGANIZATION REPORT NUMBER

N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Rome Laboratory/ERO
80 Scott Drive
Hanscom AFB MA 01731-2909

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

RL-TR-95-279

11. SUPPLEMENTARY NOTES

Rome Laboratory Project Engineer: Maxwell Chi/ERO/(617) 377-2225

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This report describes the development of $Si/Si_{1-x}Ge_x$ heterostructures for platinum silicide Schottky barriers with a cutoff wavelength of 10 microns or longer. The details of the required conditions for the growth of these heterostructures by Rapid Thermal Chemical Vapor Deposition are first described, with particular attention paid to the growth temperature, germanium content, and doping. The experimental performance of PtSi Schottky barrier detector structures is then described. The cutoff wavelength can be extended to 10 um as hoped but, in present devices, a reverse bias of several volts is needed to achieve this long wavelength, with a larger parasitic barrier present at smaller biases. Two models for this tunable barrier height are presented. It is concluded that a parasitic barrier at the lower SiGe/Si interface, coupled with a high n-type background doping, is probably responsible for the extra barrier. The required conditions for eliminating this effect are described.

14. SUBJECT TERMS

Silicon-germanium, Infrared detection, Schottky barrier detectors, Chemical vapor deposition

15. NUMBER OF PAGES

36

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Contents

1 Introduction

PtSi infrared detector arrays are the most widely used technology for focal plane arrays for the medium wavelength infrared (3-5 micron) atmospheric window band. They are successful because the readout circuitry can easily be integrated on chips, and because very good pixel to pixel uniformity which can be achieved. The long wavelength cutoff of this technology is limited to about 5.5 microns. This report describes how $Si/Si_{1-x}Ge_x$ heterojunctions can be used to extend the cutoff wavelength of PtSi detectors to 10 microns, so that they can be used for the long wavelength atmospheric window band (8-12 microns). The growth of the materials by Rapid Thermal Chemical Vapor Deposition is described in detail, and the background and physics of the new detector structure are described. Experimental results focussing on the bias dependence of the photoresponse are described. A 10 micron cutoff can be achieved, but only with a few volts of reverse bias. The probable cause for this effect is examined, and how it can be avoided is discussed.

2 $PtSi/Si_{1-x}Ge_x/Si$ IR detectors

The cutoff wavelength of PtSi/Si Schottky barriers is limited by the barrier height of about 250 meV between the Fermi level in PtSi and the valence band in Si. It has been known for several years, however, that the valence band in a strained $Si_{1-x}Ge_x$ alloy on a (100) Si substrate lies substantially above that in the Si. Therefore according to the Schottky model, one would expect a lower barrier between PtSi and the strained SiGe alloy than between PtSi and Si. This is the basis of the expected longer wavelength performance of the $PtSi/Si_{1-x}Ge_x$/Si-substrate detectors (Fig. 1). The valence band offsets between Si and strained $Si_{1-x}Ge_x$ are about 70 meV for dectectors of $PtSi/Si_{0.9}Ge_{0.1}$ and about 140

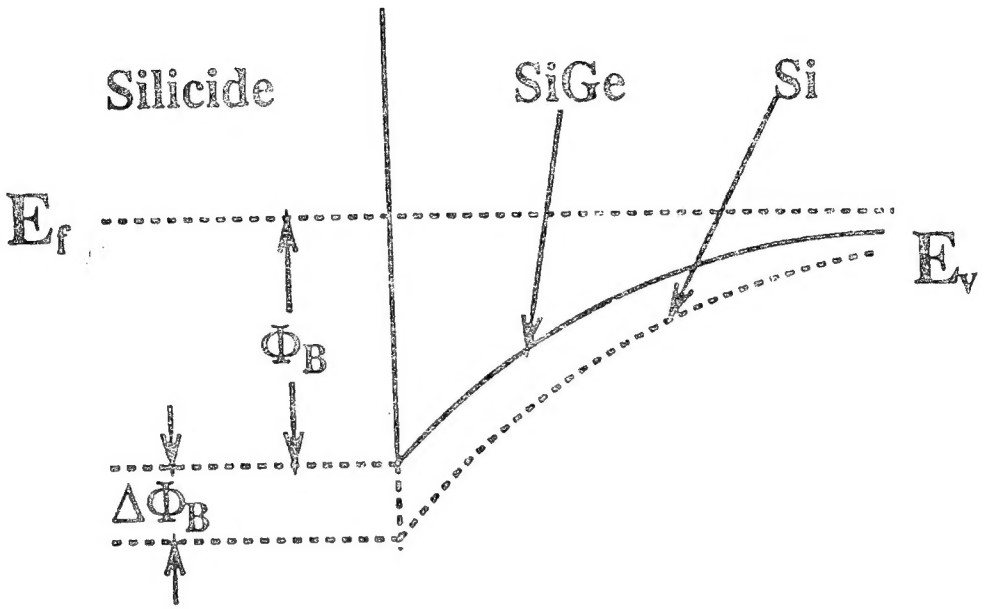


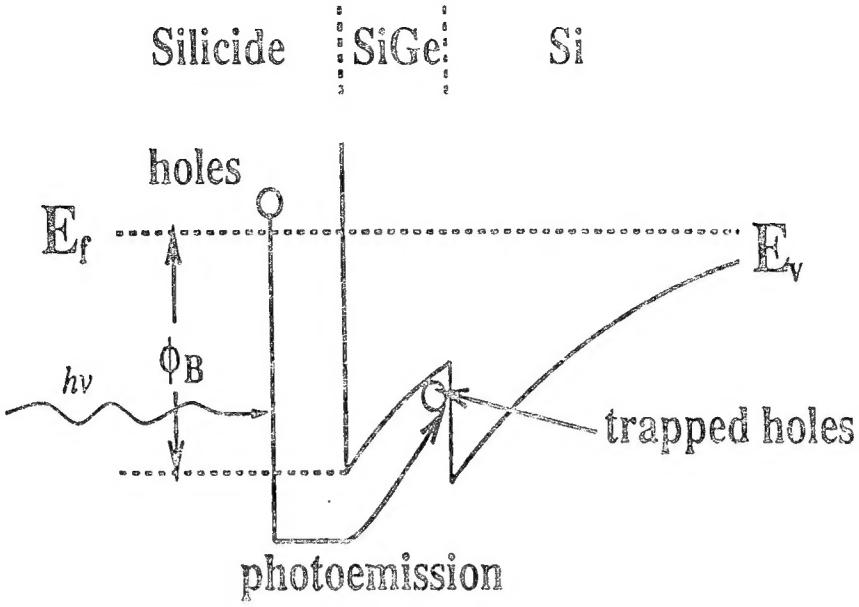
Figure 1: Band diagram of a detector with a graded lower SiGe/Si interface to avoid the formation of an abrupt parasitic valence band barrier for holes.

meV for detectors of $PtSi/Si_{0.8}Ge_{0.2}$ to have barrier heights 180 and 110 meV, respectively, corresponding to cutoff wavelengths of approximately 7 and 11 μm, respectively.

The thickness of strained SiGe is limited because of the accumulated elastic energy in the films. A typical upper limit to the thickness of $Si_{0.8}Ge_{0.2}$ is on the order of 50 nm in practice. Since this is much less than the typical thickness of the depletion region of the Schottky barrier, one must consider the effect of the $Si_{1-x}Ge_x$ /Si interface. If this were an abrupt interface, it would cause a parasitic barrier for holes travelling on their way to the substrate after being emitted from the PtSi. To avoid an abrupt barrier in these detectors, the lower $Si/Si_{1-x}Ge_x$ interface is graded as shown in Fig. 2. The exact design of this grading is fairly complicated, however, and even if no abrupt barrier exists, this interface can still present a barrier which limits the overall photocurrent. This phenomenon will be explored in detail later in this report.

PtSi is usually formed by reacting Pt with Si. In the case of SiGe, the reaction with metals is known to create defects which in some cases can pin the Fermi level and lead to higher barrier heights [1]. Therefore in our experiments we have placed a thin silicon sacrificial layer on top of the $Si_{1-x}Ge_x$ before the deposition of the metal. This silicon should be chosen so that it is exactly consumed by the silicide formation reaction. Initial experiments demonstrating the concept of using $Si_{1-x}Ge_x$ to reduce the barrier height of silicide detectors were shown by Xiao et al in Ref. 2. These experiments used $PdSi_2$, which has a barrier height to Si of 0.45 eV. Detectors with $x = 0.2$ and $x = 0.35$ exhibited a barrier height reduction of 0.11 and 0.19 eV (Fig. 3), roughly in line with expectations based on known valence band offsets.

One undesirable complication of the sacrificial Si layer is the extreme control required to maintain optimum detector characteristics. It was mentioned earlier that any metal reaction with the $Si_{1-x}Ge_x$ should be avoided. On the other hand, if the metal is too thin or if the



Solution : graded SiGe layer

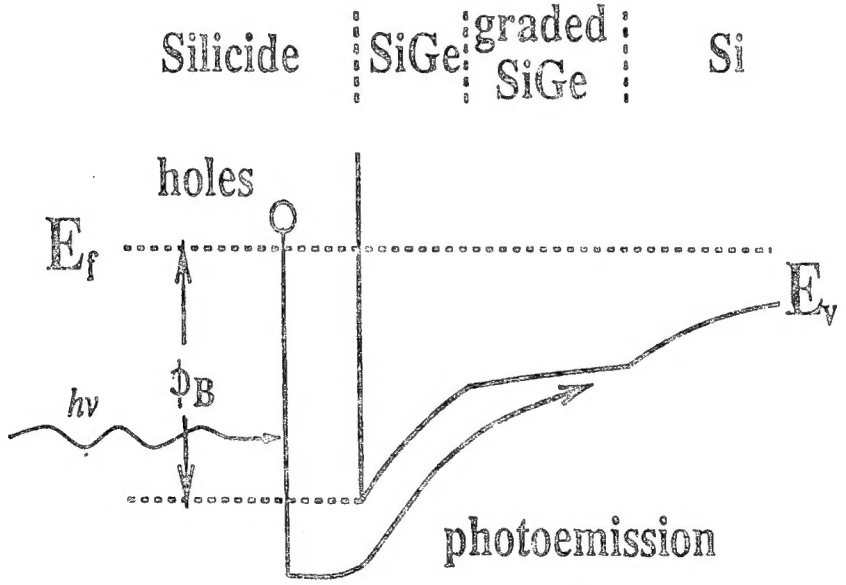


Figure 2: Band diagram of a detector with a graded lower SiGe/Si interface to avoid the formation of an abrupt parasitic valence band barrier for holes.

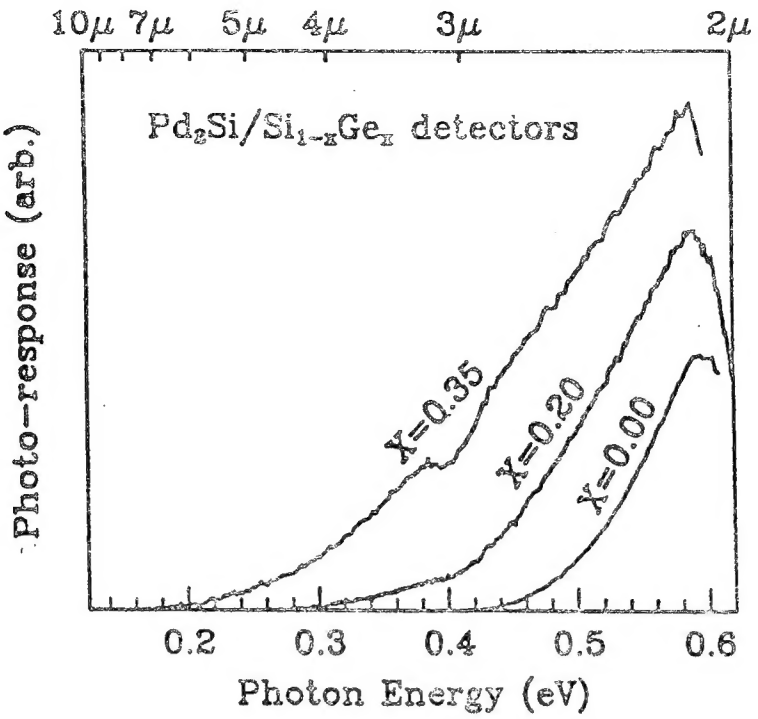


Figure 3: Initial results of $PdSi_2/Si_{1-x}Ge_x/Si$ IR detectors showing a reduction in barrier height as Ge is added.

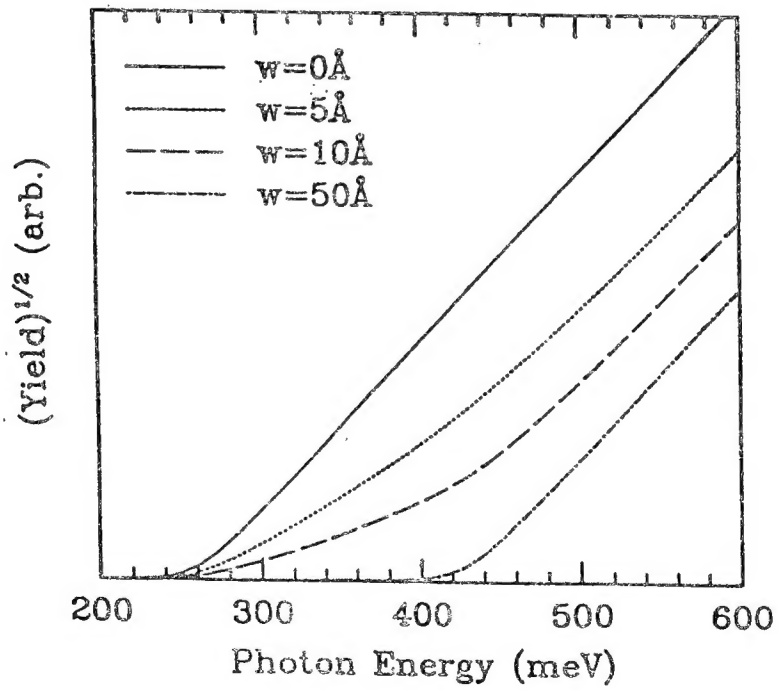


Figure 4: Calculated Fowler plot showing the effect of a thin leftover Si sacrifical layer on the photoresponse of $PdSi_2/Si_{0.8}Ge_{0.2}/Si$ infrared detectors (from Ref. 3.).

Si is too thick, a layer of unreacted Si will remain. This Si will present another barrier for the photoemitted holes. If the Si is thick, the detector performance will revert to that of a Si detector. If the remaining Si is thin, holes may be able to tunnel through the extra barrier, so that the detector has a reduced efficiency for low photon energies. The results of a simple calculation of this effect for a $PdSi_2$/Si(parasitic)/ $Si_{1-x}Ge_x$ /Si structure are shown in Fig. 4 [3].

Note that a significant degradation of performance at long wavengths is already seen for parasitic Si thicknesses as small as 0.5 nm. A more detailed calculation yields similar results [4]. Since it may be difficult to control deposition thicknesses on this scale over large wafer areas, a technology for silicide formation which does not require the consumption of a silicon layer, such as codeposition of Pt and Si, would be a very desirable direction for future research.

3 Temperature, Doping, and Germanium Control in Rapid Thermal Chemical Vapor Deposition

3.1 Rapid Thermal Chemical Vapor Deposition

All samples used in this study were grown by Rapid Thermal Chemical Vapor Deposition (RTCVD) in a reactor schematically pictured in Fig. 5. A single three- or four-inch silicon wafer is suspended on quartz pins inside a quartz tube, and the wafer is heated by tungsten halogen lamps outside of the quartz chamber. The wafer is loaded into the chamber through a load-lock so that the chamber is not vented to atmosphere when samples are exchanged. Both the main chamber and the load chamber are pumped by rotary vane pumps. The

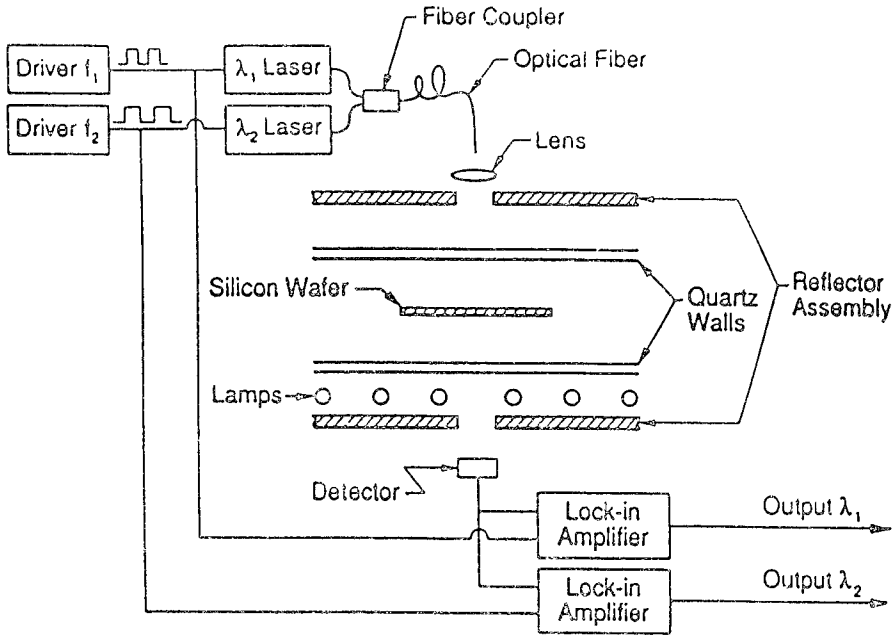


Figure 5: Cross sectional schematic veiw of the RTCVD reactor used in the experiments

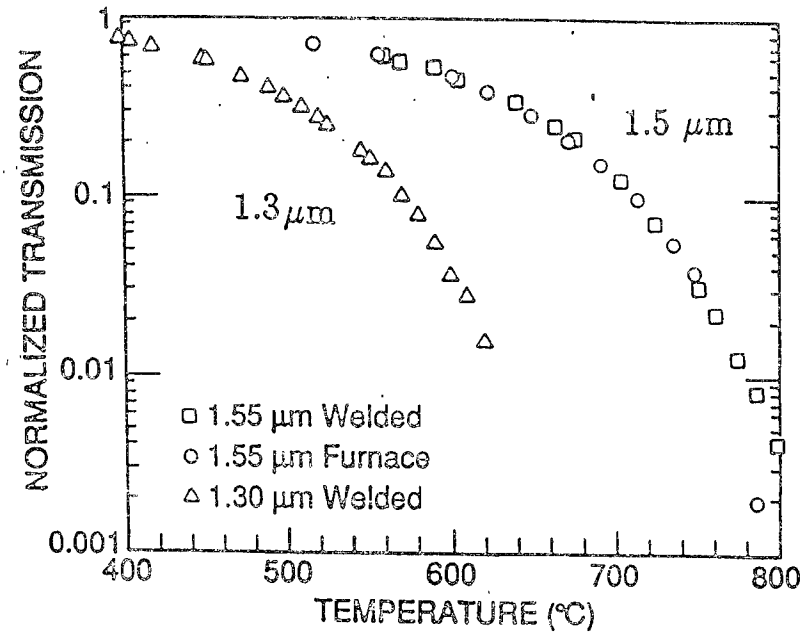


Figure 6: Normalized transmission vs. temperature for 1.3 μ m and 1.55 μ m radiation for a 500-μ m thick lightly doped silicon wafer.

growth gases for this work were dichlorosilane and/or germane (0.8 % in a hydrogen carrier), and dilute diborane (10 ppm in hydrogen) was used as a p-type dopant. Extreme care is taken regarding the purity of the gases, and the hydrogen is purified using either a Pd cell or a chemical filter (e.g. Nanochem) to remove oxygen and water vapor. Typical growth temperatures are 1000°C for a silicon buffer on the substrate (when the device structure allows it), 625 or 700°C for $Si_{1-x}Ge_x$ layers, and 700 - 800°C for critical Si device layers. The gas flow conditions were 3 lpm of hydrogen and 26 sccm of dichlorosilane and the growth pressure was 6 torr for all work in this project. Further details can be found in Ref. 5.

3.2 Temperature Measurement

Because of a desire for metastable $Si_{1-x}Ge_x$ layers above the equilibrium critical thickness, and because of a desire to avoid 3-D non-planar growth, it is generally desired to grow the $Si_{1-x}Ge_x$ layers at a temperature under 700°C. However, below 800°C CVD growth rates for Si and for $Si_{1-x}Ge_x$ layers with small x decrease exponentially as the temperature is decreased, with an activation energy on the order of 2 eV. For the gas flow conditions given above, the Si growth rate is about 30 nm/min at 800°C, and about 3 nm/min at 700°C, and under 1 nm/min at 600°C. Therefore, very precise control of the wafer temperature is required. This is historically very difficult in a rapid thermal processing chamber because of the non-equilibrium environment, and because the lamp interference and changing emissivity make pyrometery difficult.

Therefore we measure the wafer temperature by measuring the infrared absorption of the silicon substrate in situ in the reactor (Fig. 5). Because of the decrease of the bandgap and the increase of the free carrier concentration with temperature, both bandgap and free carrier absorption increase rapidly with temperature. The absorption at wavelengths of 1.3 and 1.55 μm are especially sensitive in the 500 - 800°C range which is relevant for this work.

These wavelengths are provided by semiconductor lasers which are modulated at moderate frequency (10 KHz) so that lock-in techniques can be used to distinguish the transmitted laser radiation from interference from the lamps [6-7]. By dividing the high temperature transmitted signal from the room temperature signal (where the absorption is a minimum) a normalized transmission signal is obtained which is independent of laser power, detector efficiency, and also of any scattering of the laser beam off the wafer backside (which is not a function of temperature). Fig. 6 shows the strong dependence of this normalized transmission on temperature.

One might be concerned about the effect of $Si_{1-x}Ge_x$ layers on the transmission through the substrate. Modelling shows that this is not a concern for layers with $x < 0.5$ and thinner than 1 μm. This was experimentally confirmed for the case of $x = 0.33$ and a layer thickness of 27 nm on each side of a wafer by measuring the transmission vs temperature (using a thermocouple embedded in the wafer to measure temperature) both before and after the $Si_{1-x}Ge_x$ growth (Fig. 7) [8]. Within the experimental error, there was no discernable difference in the normalized transmission after the $Si_{1-x}Ge_x$ layer was grown.

3.3 $Si_{1-x}Ge_x$ Growth Conditions

As mentioned earlier, it is desirable for several reasons to grow the $Si_{1-x}Ge_x$ layers at temperature at or under 700°C. Under 700°C, however, the growth rate of Si for the gas conditions used in this work was prohibititively slow. Fortunately, the growth rate of SiGe alloys is substantially larger than that of Si at low temperatures. For example, with a flow of 100 sccm of 0.8% germane in hydrogen added to the above conditions, a growth rate of 10 nm/min at 625°C of $Si_{0.8}Ge_{0.2}$ results.

Because the growth rate of the $Si_{1-x}Ge_x$ layers depends not only on temperature but also on the germanium fraction (through the germane flow), SIMS was performed on a

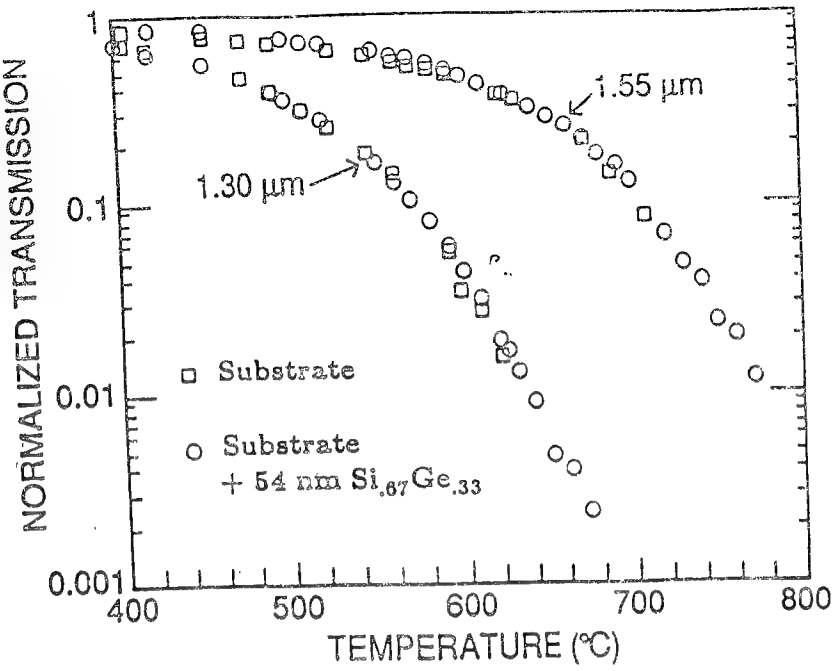


Figure 7: Normalized transmission at 1.3 and 1.55 μm for the wafer of Fig. 6 with and without 54 nm of $Si_{0.7}Ge_{0.3}$ on the surface, showing the insensitvity of the temperature measurement technique to thin SiGe surface layers.

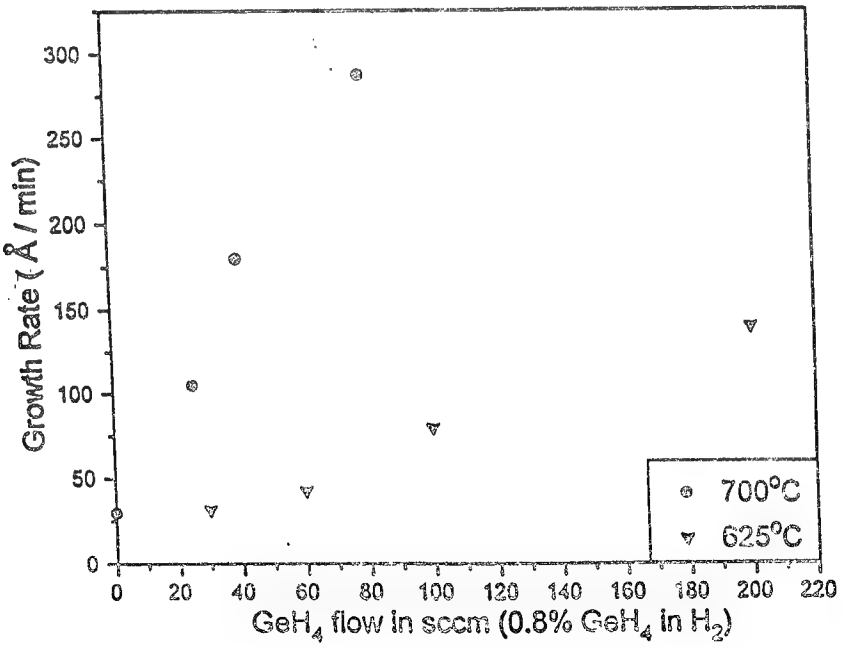


Figure 8: Growth rate vs. germane flow (.8% flow of 3 lpm, dichlorosilane flow of 26 sccm), pressure of 6 torr and temperatures of 625 and 700°C.

multilayer sample with various germane flows at 625 and 700°C to determine the growth rate for various flow conditions. The results for the growth rate and germanium fraction x are shown in Figs. 8 and 9. Because the growth rates under 700°C are still small for x < 0.1, layers with x of 0.1 or less were grown at 700°C, while layers with x over 0.1 were grown at 625°C. Graded layers were grown either in a staircase fashion or with the Ge continously ramped. Because the growth rate is a function of germane flow, to try to achieve a linear grading in germanium fraction, the rate of change of the germane flow in this case was occasionally changed. Because the residence time of gases in the chamber is on the order of 5 sec, and because the growth rates were on the order of 5 nm/min or so, graded layers with gradings sharper than 10% Ge in about 10 nm could not be accurately controlled.

Due to the presence of Cl in dichlorosilane, selective Si growth can be achieved under the above growth conditions from 700 to 1000°C without the addition of extra HCl. However, this requires that there be no trace amounts (less than ppm) of water vapor or oxygen in the gas streams [9], as is usually achieved in our system. The growth of $Si_{1-x}Ge_x$ is also selective for thin layers of temperatures of 625 or 700°C without any changes in the growth conditions.

3.4 Doping

Ideally PtSi Schottky barrier IR detectors have a light p-type doping (e.g. 10^{14} cm^{-3} - 10^{15} cm^{-3}). Heavier doping leads to higher electric fields which can decrease Schottky barrier due to classical image force effects, and also to tunneling. In principle, p-type doping in low temperature Si or $Si_{1-x}Ge_x$ CVD is straightforward since there are no parasitic effects such as autodoping, surface segregation of the dopant, etc. Furthermore, it has been established that the incorporated boron level is proportional to the diborane partial pressure over many orders of magnitude, and that the boron is fully electrically active to levels in excess of

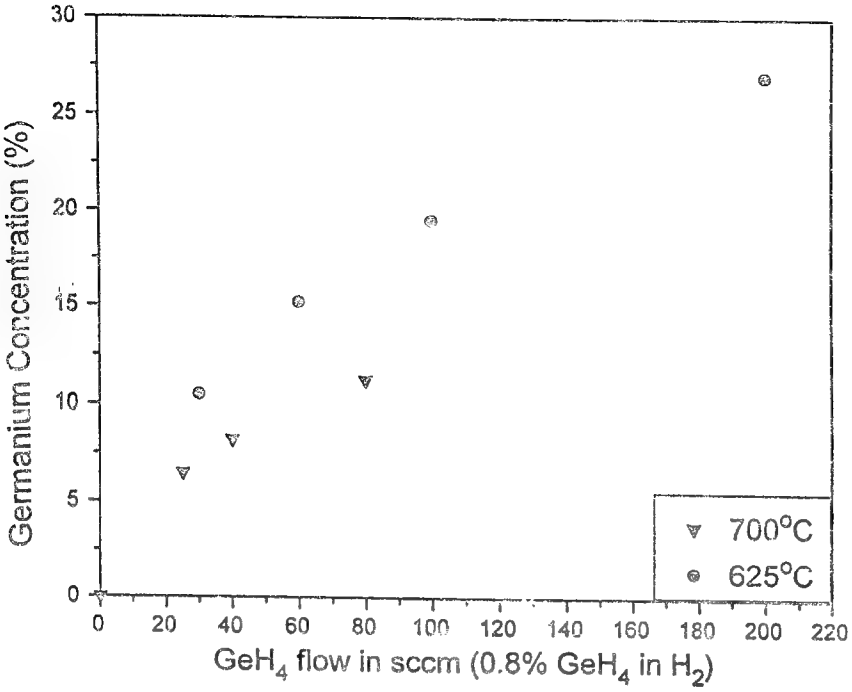


Figure 9: Germanium fraction for the growth conditions of Fig. 8.

Growth Temperature (C)	Germane Flow (sccm)	x (Ge content)	Diborane Flow (sccm)	Boron Concentration (cm^3)
625	200	0.27	10	3×10^{17}
625	60	0.15	10	4×10^{17}
700	80	0.12	10	7×10^{16}
700	25	0.06	10	2×10^{17}
1000	0	0	10	3×10^{16}
1000	0	0	100	3×10^{17}

Figure 10: Boron doping levels for various germane, temperature, and dibornae (nominally 10 ppm) conditions. Other conditions were 26 sccm dichlorosilane, 3 lpm hydrogen, and 6 torr.

10^{20} cm^{-3}.

In practice, several factors make it difficult to accurately achieve low doping levels. First, the boron incorporation ratio depends on growth rate. Therefore a multilayer sample was grown for SIMS analysis to measure doping levels under various growth conditions. These results are summarized in Fig. 10. The diborane source used had a "nominal" concentration of 10 ppm. However, the dopings were approximately 1 order of magnitude lower than those typically achieved in our system in the past under several of the conditions. Therefore it appears that the diborane source may have degraded over time and that the concentration was indeed much less than 10 ppm. (The stability of diborane and its mixtures is a known problem). Therefore the doping of a single growth condition must be validated when actually growing wafers, and from that single point one can then use the relative doping levels found under different conditions (found from Fig. 10) to determine appropriate flow rates.

A second practical problem is the range of doping achievable. As mentioned, doping in the 10^{14} cm^{-3} - 10^{15} cm^{-3} range is desirable for the active region of detectors, while a more heavily doped layer under the detector may be desirable for a "substrate contact" layer, especially in test structures. A single mass flow controller has a range of flow of at most 50X however. Even if two are placed in parallel, the smallest achievable flow is about 0.5 sccm in practice, and the largest flow (without grossly affecting growth conditions) is about 1 lpm. Since the doping is proportional to the diborane partial pressure (and hence flow), a maximum doping range of only 200 X results if one uses a single tank of a doping source. To achieve a wider range, one must use a dopant dilution system in the gas supply system, where the dopant source can be futher diluted before being metered for flow into the reactor. Therefore it would be highly desirable for future IR detector work if such a dopant dilution system was incorporated into the dopant supply system.

A last practical issue is that of compensation. The n-type dopant used in the existing

reactor is phosphine. Because phosphine is very hard to remove from quartz walled systems to very low pressure, and because of the large sticking coeficient of phosphine on silicon surfaces at low temperatures, there is a problem in the existing reactor with memory effects. Several wafers after the growth of a n-type layer using phosphorus, the background concentration of "undoped" layers grown can still be on the order of 10^{18} cm^{-3}. This number can be reduced by baking and repeated growths, but in any case it is very difficult to achieve reliable doping at levels under 10^{17} cm^{-3}. Arsine does not exhibit tendencies as bad as phosphine regarding memory effects. Further, HCl etching at high temperature is known to be very useful for greatly reducing memory effects. However, HCl is not available on the current reactor. Therefore it is recommended that HCl etching be available on any reactor used for future work, and also that arsine perhaps be substituted for phosphine.

4 Experimental Results and Interpretation

4.1 Device Structure

Some of the measurements for this project were performed on a device with a cross section shown in Fig. 11. Heavily doped p^+layers (for a substate contact) were first grown on a p-type substrate, followed by a nominally undoped silicon layer at 1000°C. It was hoped that autodoping at high temperature would dope these regions p^-, although this was not confirmed. After the blanket epitaxial layers, an oxide was grown and an n^+guard ring layer was implanted. This was annealed in oxygen, and a window for selective epitaxy was then opened by wet etching. In this hole a $Si_{1-x}Ge_x$ graded layer was grown, followed by a uniform $Si_{1-x}Ge_x$ layer. The graded layer thicknesses were on the order of 10-30 nm, and the uniform layer thicknesses were 30-60 nm (grown at 625°C) for a final x of 0.15 and 0.20,

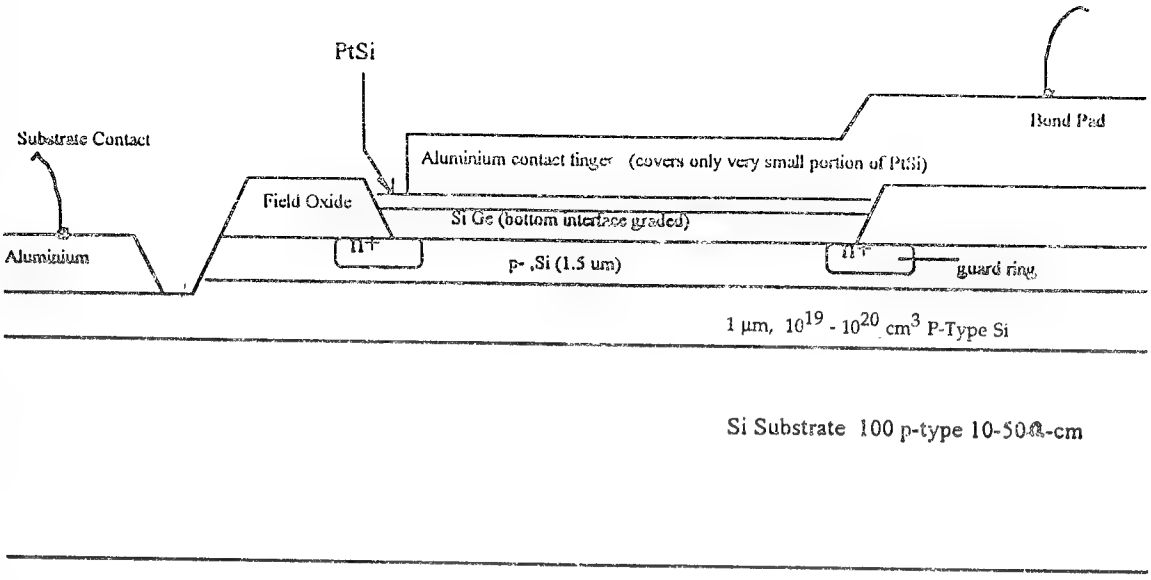


Figure 11: Device structure incorporating a guard ring and selective epitaxial growth.

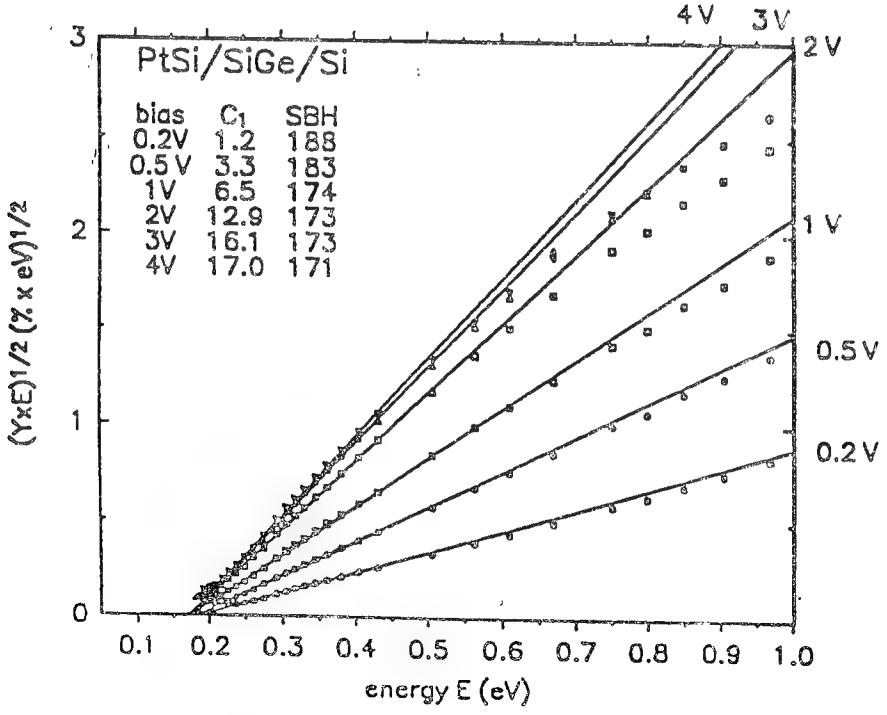


Figure 12: Fowler plots of a device with a final Ge fraction of 0.10

and 60 - 120 nm (grown at 700°C) for a final x of 0.05 and 0.10. The final germanium fractions were nominally 0.05, 0.10, 0.15, and 0.20, in addition to a control sample with no selective $Si_{1-x}Ge_x$ layer. On top of the $Si_{1-x}Ge_x$ a sacrificial Si layer of 4 nm was grown. Pt evaporation and and subsequent annealing for silicide formation (and removal of the unreacted Pt) were performed at the David Sarnoff Research Center. A trench was cut to contact the buried p^+layer, and aluminium metallization completed the processing (for contacting the p^+layer and the silicide.)

Other measurements were performed on devices formed without guard rings or selective epitaxy. In this case the $Si_{1-x}Ge_x$ layers were grown directly on top of the high temperature buffers layers without removing the wafers from the growth chamber. The gradings and thicknesses were similar to those described above. On some samples the Si sacrificial layer was intentionally omitted to probe the effect of reacting the metal directly with the $Si_{1-x}Ge_x$. The metal, which was usually Pt although Ir was used in a few cases, was evaporated though a shadow mask and annealed in situ at Rome Lab.

4.2 Photoresponse

The devices rectified with the proper polarity at low temperatures. Photoresponse measurements as a function of applied bias were made at Rome Lab. The temperature was between 20 K and 40 K, with no strong temperature dependence within this range. The device results fell into three different classes. First, the devices without Si caps had barrier heights larger than those of Si control samples. This occured both for Ir and Pt silicides. This is consistent with the concept of defect formation occuring when the metals react with SiGe [10, 4].

When a sacrificial Si cap was included, the devices with germanium fractions of 0 (no Si cap in this case), 0.05, and 0.10 had photoresponses which looked similar to those of all-Si devices, although shifted to longer wavelength as Ge was added. Typical Fowler plots are

shown in Fig.12. Note that although the barrier height had little dependence on bias, similar to the control device, the C_1 factor had a strong dependence on bias (Fig. 13). This suggests an excessively low scattering length for the holes in the $Si_{1-x}Ge_x$. The cause of this has not been investigated in detail. Note that the barrier height reduction compared to the all-Si device is about 50 meV, which is smaller than the 70 meV expected for a germanium fraction of 0.10. This may be due to the actual Ge fraction being lower than desired.

The most interesting results were obtained for Ge fractions of 0.15 and 0.20. A typical set of Fowler plots is shown in Fig. 13. In these cases at low bias the barrier height was excessively large (larger than that of an all-Si device), and the C_1 coefficients were on the order of only 1%/eV (about 10 times lower than a good all-Si device). As the reverse bias was increased, however, the barrier height fell sharply and the C_1 coefficient increased sharply (exceeding 20%/eV for the $x = 0.15$ device). Note that the barrier height lowering saturated with several volts of reverse bias. This fact will be important in discriminating between models in the next section of this report. The fact that the cutoff wavelength changed with bias demonstrates that the device is electrically tunable.

If controllable, this effect could be exploited in applications. The fundamental origin of this effect is explored in the next section. For the $x = 0.2$ devices, for several volts of reverse bias the barrier heights are on the order of 110 - 120 meV (corresponding to cutoff wavelengths of 10 - 11 μm). Thus a key goal of this project was achieved.

4.3 Tunable Detector Physics

4.3.1 Defect Model and Schottky Barrier Lowering

Two basic phenomena can be used to explain the observed characteristics of a large barrier at small bias and a small barrier at large bias. The first model invokes both interfacial

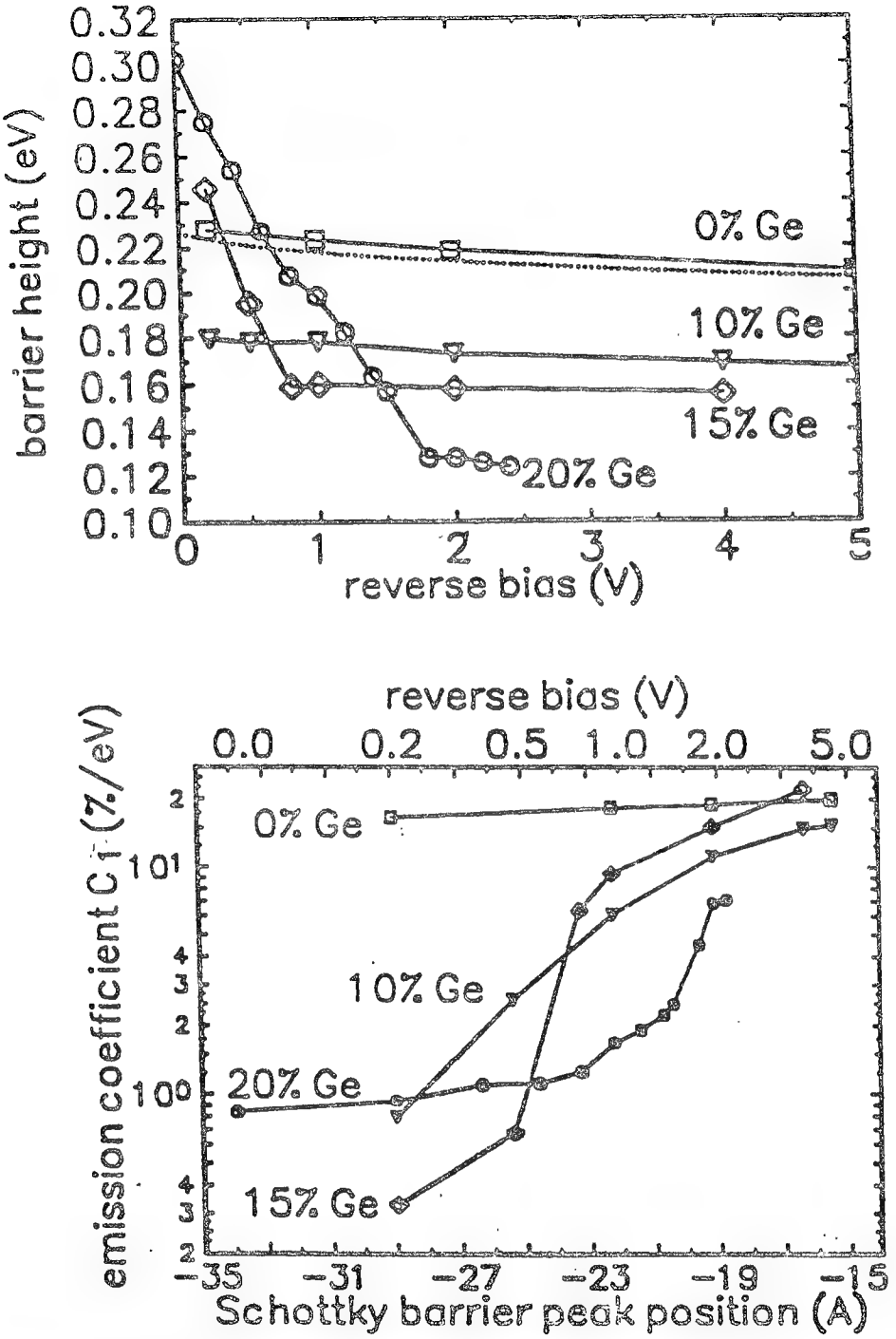


Figure 13: Dependence of barrier height and emisison coefficient (C_1) extracted from Fowler plots for various final Ge fractions.

defects and heavy p-type doping. It has already been established that reaction of the metal with the $Si_{1-x}Ge_x$ can in some cases lead to a larger barrier formation because of defect formation. A large number of defect levels near the center of the bandgap will tend to pin the Fermi level near midgap, leading to a larger barrier height. Applying a reverse bias can reduce the effective barrier height through barrier lowering mechanisms. Conventional image force lowering is too small to account for the large shifts seen in Fig. 13 (100's of meV with only a few V of bias), but if heavy p-type doping were present, tunneling could cause the barrier height to be a strong function of bias. Transmission Electron Microscopy (TEM) was performed at Princeton on one detector which had the PtSi formation process performed at the David Sarnoff Research Center. The sacrificial Si layer target thickness was 4 nm, and the desired Pt evaporation thickness was 2.5 nm for final PtSi thickness of 5 nm. However, TEM showed a PtSi thickness of 8 nm in the sample. This would imply that the evaporated Pt thickness was too high, and that some 2-3 nm of $Si_{1-x}Ge_x$ reacted with the Pt. This evidence tends to support this model as the origin of the tunability. However, the fact that the barrier height lowering saturates with several volts of reverse bias is difficult to explain with this model.

4.3.2 Parasitic Barriers

A second model of tunability can be invoked if one recalls that a parasitic barrier may occur at the lower $Si/Si_{1-x}Ge_x$ interface. It was earlier discussed that grading may eliminate an abrupt valence band barrier (e.g. Fig. 2.), but even in the presence of grading the valence band may be substantially lower at the lower $Si/Si_{1-x}Ge_x$ interface than at the $PtSi/Si_{1-x}Ge_x$ interface. Fig. 14 shows the zero-bias band diagram in a typical detector structure with a final Ge fraction of 0.15, and graded and constant Ge layers of 30 nm each. Note that if the doping is low, so that the band bending is gradual, the valence band at the

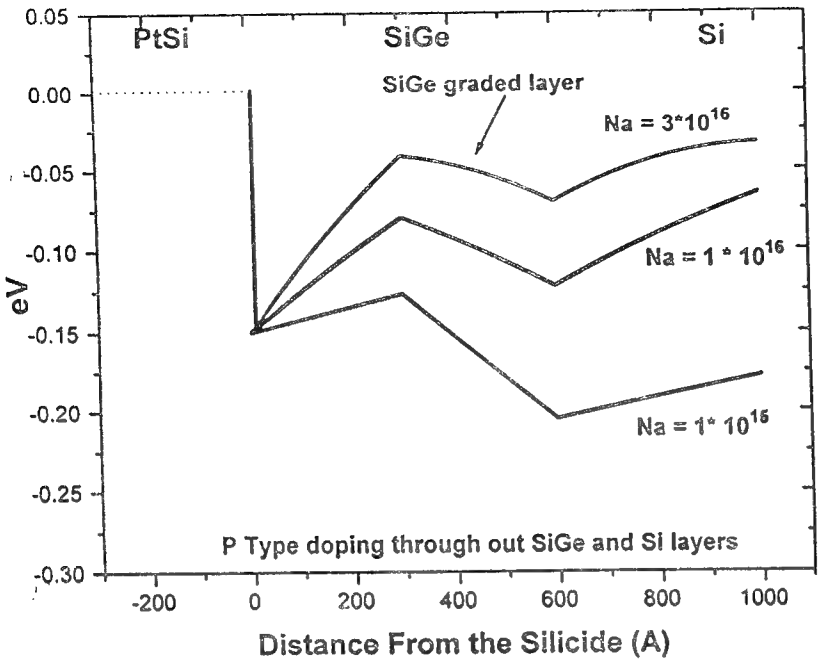


Figure 14: Band diagram at zero bias for various uniform p-type dopings. 30 nm graded and constant $Si_{1-x}Ge_x$ layers were assumed, with a final x of 0.15.

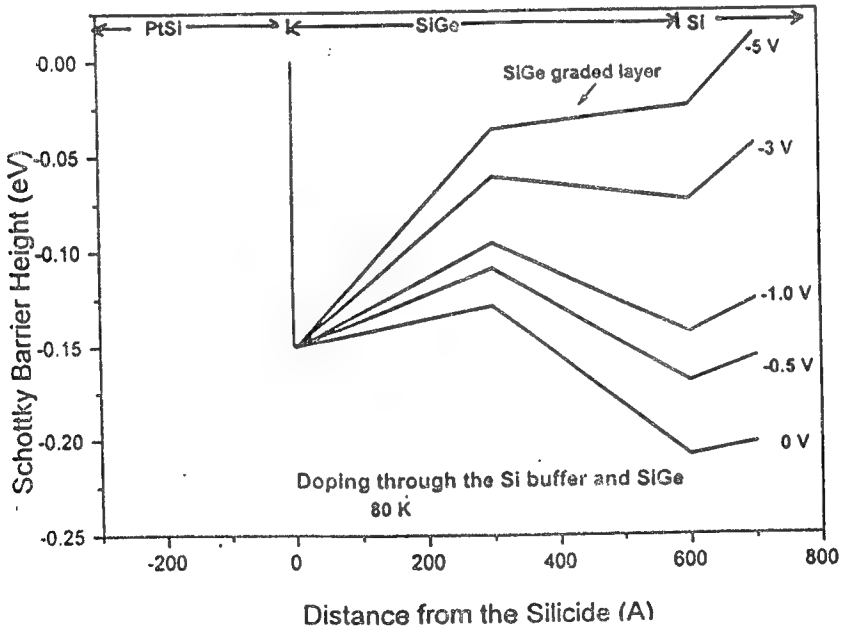


Figure 15: Band diagram at several reverse biases for the structure of Fig. 14 with a doping of $1 \times 10^{15} cm^{-3}$. Note the reduction of the total barrier faced by a hole from the PtSi.

lower $Si/Si_{1-x}Ge_x$ interface will indeed be much lower than the valence band of the metal interface. Therefore a hole with much larger energy than the Schottky barrier height will be required to get across this extra barrier. Further, the long distance of this barrier from the metal would explain the extemely low C_1's observed for small reverse biases.

As the reverse bias is increased, the parasitic barrier will be pulled up, so that the barrier height would be reduced. This is consistent with the observed data for x = 0.15 and 0.20 in Fig. 13. Finally, after some level of reverse bias, the parasitic barrier is raised to the point where it is now higher than the valence band at the metal interface, so it no longer plays a role in the transport of holes from the metal to the semiconductor (Fig. 15). In this case the barrier height measured by photoresponse would depend simply on the true Schottky barrier, and would become constant at the value expected from the higher valence band in SiGe, independent of any parasitic barrier effects. Indeed such a saturation of the barrier height is observed in the barrier height measurements as a function of bias (Fig. 13). This is very strong evidence in favor of the above model. Furthermore, at a reverse bias for which the parasitic barriers are removed, a good agreement is achieved between the measured barrier heights and those expected based on known valence band offsets between Si and $Si_{1-x}Ge_x$ (Fig. 16).

To avoid the formation of a parasitic barrier, it is obvious from Fig. 14 that one needs either very thick $Si_{1-x}Ge_x$ layers or a doping in excess of 10^{16} cm^{-3}. Even in the case of 3×10^{16} cm^{-3} in Fig. 14, a "trap" for holes at the constant $Si_{1-x}Ge_x$ /graded $Si_{1-x}Ge_x$ interface exists, which may adversely affect device operation. Achieving thicker $Si_{1-x}Ge_x$ layers is limited by the strain of these layers which results from their natural lattice mismatch to Si. Therefore a very important direction of future work would be to develop heterojunction systems to Si which have a lower level of strain (for a similar bandgap offset) so that thicker layers may be allowed. SiGeC alloys are one very promising material for this

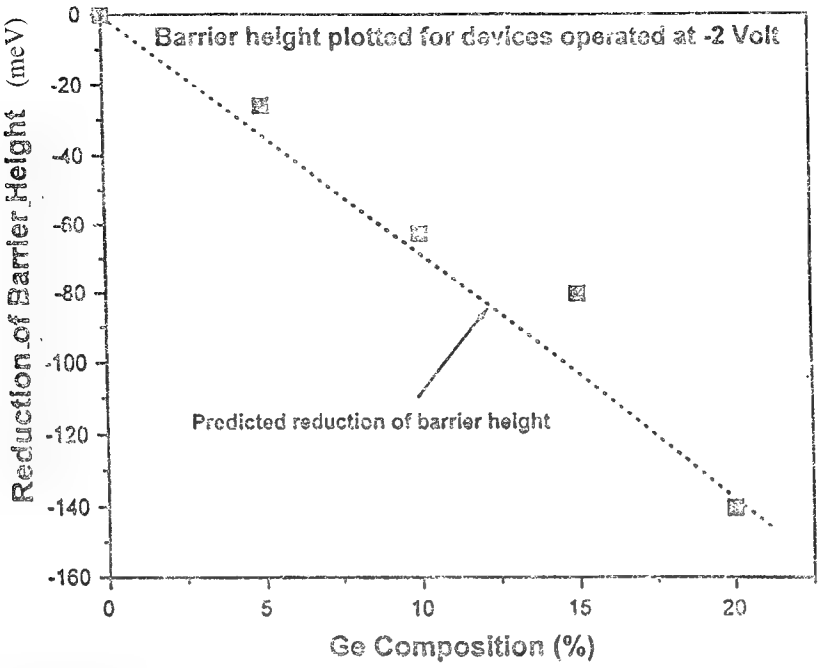


Figure 16: Experimentally measured barrier height (Fowler plot) at 2 V reverse bias a function of final Ge fraction.

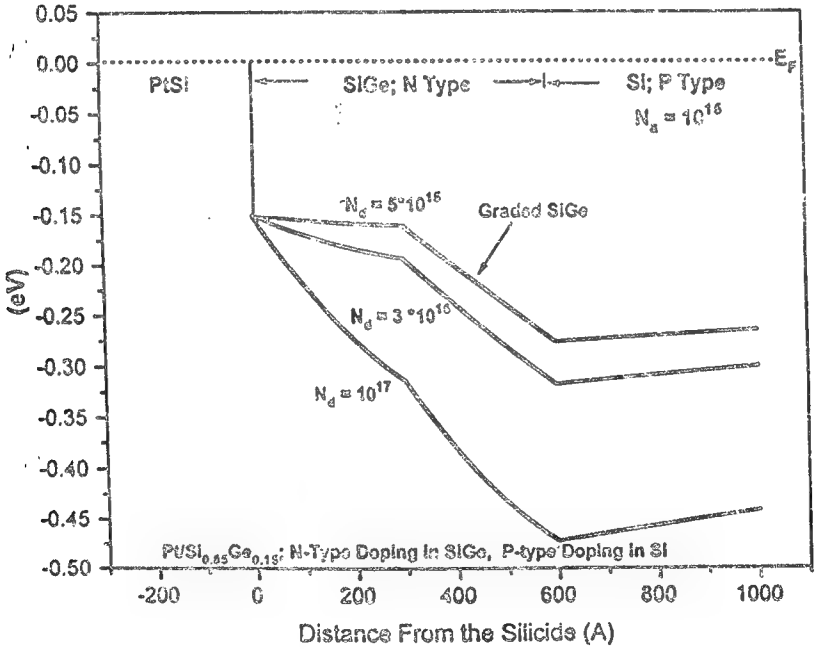


Figure 17: Band diagram at zero bias for a structure similar to that of Fig. 14, with p-type doping of 1×10^{15} cm^{-3} below 60 nm from the surface, but with n-type dopoing in the top 60 nm. Note the total barrier face by holesw at zero bias exceeds 250 meV.

purpose.

As presented to this point, one serious objection to the parastic barrier model can be raised. In a structure which is doped everywhere p-type, the largest barrier which can be observed is that of PtSi/Si (about 250 meV). This can be seen by extrapolating the valence band lines of the Si substrate to the PtSi/SiGe interface in Fig. 14. Experimentally, however, barrier heights in the tunable structures as large as 0.30 eV are observed. This objection can be overcome if one hypothesizes that due to poor dopant control (and increased sticking of any background phosphine at low temperatures), some part of the near surface structure were n-type instead of p-type. If the n-type doping were heavy or the n-layer were thick, one would have a regular p-n junction and no IR response. However, if the n-type doping were light and/or the layer were thin, a structure like a camel diode would result. That is, the n-type doping could cause the bands to initially bend down as one moved away from the metal (instead of up), with the possible result that the total hole barrier at zero bias in a PtSi/$Si_{1-x}Ge_x$ /Si structure would be larger than that at the PtSi/Si interface. This is shown for several n-type dopings (for the top and graded $Si_{1-x}Ge_x$ layers only) in Fig. 17. Note for an n-type doping of 3×10^{16} cm^{-3}, a total barrier height of about 0.33 eV at zero bias would result. As in the case of an all p-type structure, applying a reverse bias removes the effect of the parasitic barrier (Fig's. 18, 19). The qualitative similarity of the simulation results of Fig. 19 and the data of barrier height vs. bias (Fig 13) is again strong evidence for the parasitic barrier model, in this case with a slightly n-type layer present.

Note that this tunability was seen for $x = 0.15$ and $x = 0.20$ (which were grown at 625°C), but not for $x = 0.10$ or less (grown at 700°C). This is consistent with the fact that background doping and memory effects (perhaps due to increased phosphine sticking coefficients) are worse at lower growth temperature. Whether or not one is interested in the tunability aspect of the detectors, it is clear that the doping of layers must be accurately

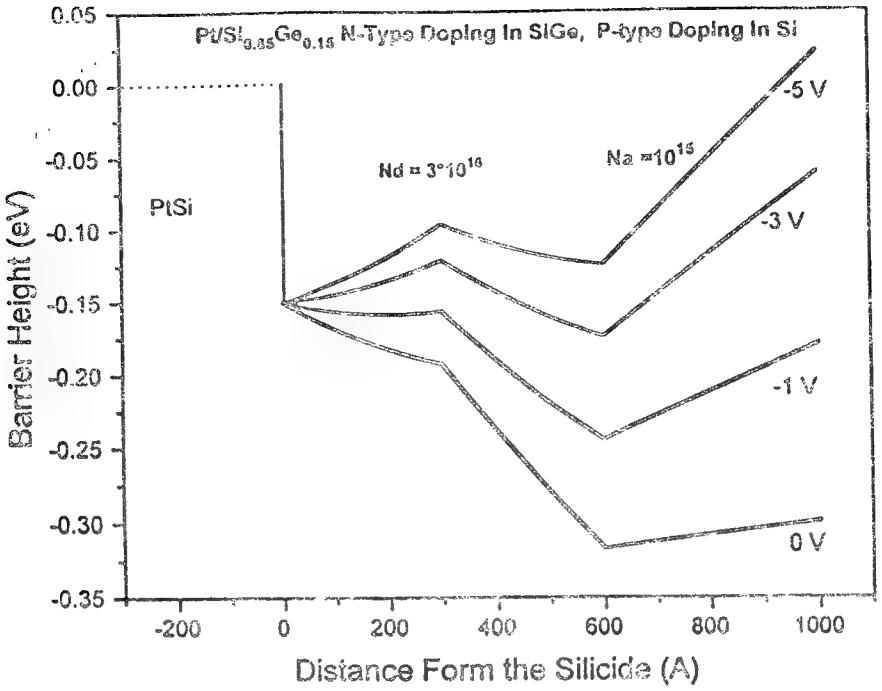


Figure 18: Band diagram of the structure in Fig. 17 with the n-type doping fixed at $3 \times 10^{16}\text{cm}^{-3}$ for several biases.

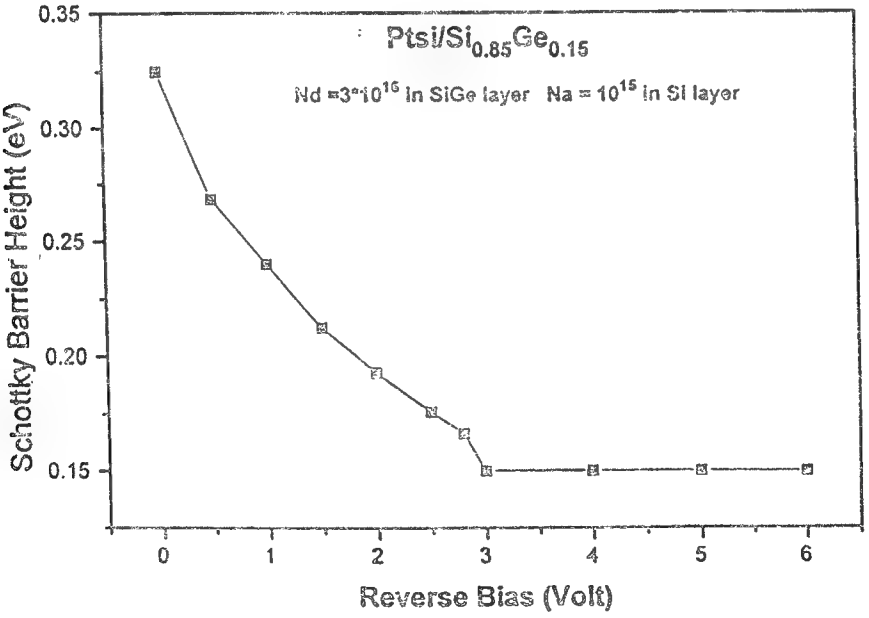


Figure 19: Total barrier height faced by holes as a function of reverse bias for the structure of Fig. 18.

controlled on the level of 10^{16} cm^{-3} or better. Such control is not possible at present in the exisiting reactor at Princeton at low growth temperatures. A new reactor is at present under construction which will have dopant dilution systems and HCl capability. These were two of the earlier recommendations for achieving better control of low doping levels.

5 Suggestions for Future Work

From this project one can propose several promising directions for future work. The first involves the accurate control of low doping levels at low growth temperatures. This has been mentioned several times in this report. A second area also mentioned earlier in the report is that of co-deposition process for Si and Pt, so that potential reactions of metal with $Si_{1-x}Ge_x$ and and complications from remaining sacrificial Si caps may be avoided. We recently have grown structures for codeposition experiments on prepatterned substrates from Rome Lab, and the devices are presently undergoing final processing at Rome Lab.

A third area of more fundamental interest involves the nature of hole transport in these $Si_{1-x}Ge_x$ Schottky barrier structures, especially hot holes. This work focussed mainly on the barrier height measured by photoresponse, and did not focus on the details of I-V curves, thermal leakage, or the details of the dependence of the emission coefficient on bias. The properties of hot hole transport at the $PtSi/Si_{1-x}Ge_x$ interface and across $Si_{1-x}Ge_x$ are especially relevant to these issues, especially in the tunable structures where the limiting barrier may be some distance from the PtSi. Furthermore, in structures with parasitic barriers, it is not clear how the optical barrier height (as measured by photoresponse) should correspond to the electrical barrier heights (measured by forward bias I-V or thermal dependence of leakage current).

Finally, these structures, like most Si-based heterostrucures, would benefit if the design

space were expanded beyond that made available by the $Si_{1-x}Ge_x$ /Si material system alone. This is especially clear in the case of the limited thickness of strained layers, since this impacts the issue of parasitic barrier formation. SiGeC alloys are one class of new materials which should be investigated to develop the next generations of Si-based heterostructure devices.

6 Refererences

1. H.K. Liou et al, Appl. Phys. Lett. 60, 577 (1992).

2. X. Xiao, J.C. Sturm, et al, IEEE Elec. Dev. Lett. 14, 199 (1993).

3. X. Xiao, J.C. Sturm, et al, J. Vac. Sci. Technol. B 11, 1168 (1993).

4. J. Jimenez et al, J. App. Phys. 75, 5160 (1994).

5. J.C. Sturm et al, J. Vac. Sci. Tech 9, 2011 (1991).

6. J.C. Sturm et al, Appl. Phys. Lett. 56, 961 (1990).

7. C.M. Reaves, et al, IEEE Trans. Elec. Dev. 39, 81 (1992).

8. J.C. Sturm et al, J. Appl. Phys. 69, 542 (1991).

9. T.O. Sedgwick, Appl. Phys. Lett. 54,2689 (1989).

10. H. Kanaya, Jap. J. Appl. Phys. 28, L544 (1989).

7 Publications Resulting from this Work

1. J.R. Jimenez, X. Xiao, J.C. Sturm, P.W. Pellegrini, and M. Chi, "Schottky barrier hieghts of Pt silicides on SiGe," *Proc. Symp. Mat. Res. Soc.*, 320, (1994).

2. J.R. Jimenez, X. Xiao, J.C. Sturm, P.W. Pellegrini, and M.M. Weeks, "Schottky barrier heights of Pt and Ir silicides formed on Si/SiGe measured by internal photoemission," *J. Appl. Phys,* 75, 5160 (1994).

3. J.R. Jimenez, X. Xiao, J.C. Sturm, P.W. Pellegrini, and M.M. Weeks, "Silicide/SiGe Schottky diode infrared detectors," *Proc. SPIE.*, 2225, 393 (1994).

4. (Invited) J.C. Sturm, A. St. Amour, Y. Lacroix, and M.L.W. Thewalt, "Luminescence in strained $Si_{1-x}Ge_x$ heterostructures," *Proc. Symp. Mat. Res. Soc.*, 379, (1995).

5. J.C. Sturm, A. St. Amour, K. Brunner, J. Weber, Y. Lacroix, and M.L.W. Thewalt, "Band-edge photoluminescence of pseudomorphically strained SiGeC layers on Si (100) substrates," presented at the Electronic Materials Conf., Charlottesville, VA, June, 1995.

6. C.L. Chang, A. St. Amour, L. Lanzerotti, and J.C. Sturm, "Growth and electrical performance of heterojunction p^+-SiGeC/p^-Si diodes," submitted to Mat. Res. Soc. Fall Meeting, 1995.

7. J.R. Jimenez, X. Xiao, J.C. Sturm, and P.W. Pellegrini, "Tunable, long-wavelength PtSi/SiGe/Si Schottky diode infrared detectors," *Applied Physics Letter,* 67 (4) (1995).

*U.S. GOVERNMENT PRINTING OFFICE: 1996-710-126-20249

MISSION

OF

ROME LABORATORY

Mission. The mission of Rome Laboratory is to advance the science and technologies of command, control, communications and intelligence and to transition them into systems to meet customer needs. To achieve this, Rome Lab:

a. Conducts vigorous research, development and test programs in all applicable technologies;

b. Transitions technology to current and future systems to improve operational capability, readiness, and supportability;

c. Provides a full range of technical support to Air Force Materiel Command product centers and other Air Force organizations;

d. Promotes transfer of technology to the private sector;

e. Maintains leading edge technological expertise in the areas of surveillance, communications, command and control, intelligence, reliability science, electro-magnetic technology, photonics, signal processing, and computational science.

The thrust areas of technical competence include: Surveillance, Communications, Command and Control, Intelligence, Signal Processing, Computer Science and Technology, Electromagnetic Technology, Photonics and Reliability Sciences.